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Renesas Electronics website: http://www.renesas.com

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# RENESAS

# HD74LS373

## Octal D-type Transparent Latches (with three-state outputs)

REJ03D0482–0200 Rev.2.00 Feb.18.2005

The HD74LS373, 8-bit register features totem-pole three-state outputs designed specifically for driving highlycapacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capacity of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was setup.

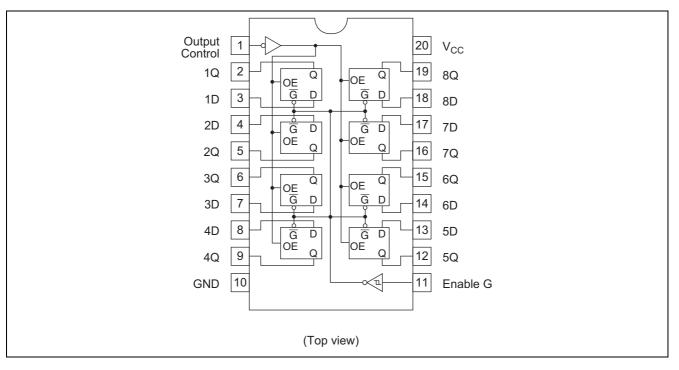
#### Features

• Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)	
HD74LS373P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	Р	—	
HD74LS373FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)	
HD74LS373RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)	

Note: Please consult the sales office for the above package availability.

### **Pin Arrangement**





#### **Function Table**

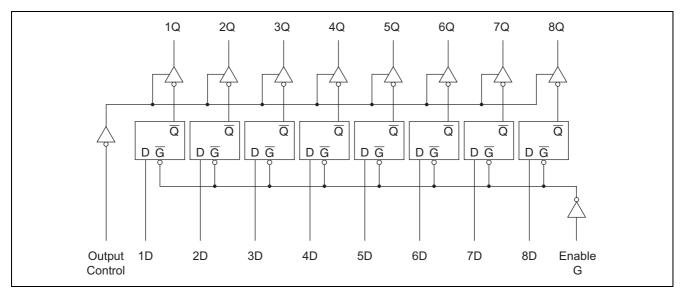
	Output		
Output control	Q		
L	Н	Н	Н
L	Н	L	L
L	L	Х	Q <sub>0</sub>
Н	Х	Х	Z

Notes: H; high level, L; low level, X; irrelevant

 $\mathsf{Q}_0\text{;}$  level of  $\mathsf{Q}$  before the indicated steady-state input conditions were established

Z; off (high-impedance) state of a three-state output

### **Block Diagram**



### **Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit	
Supply voltage	V <sub>CC</sub>	7	V	
Input voltage	V <sub>IN</sub>	7	V	
Power dissipation	P <sub>T</sub>	400	mW	
Storage temperature	Tstg	–65 to +150	°C	

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

### **Recommended Operating Conditions**

Item		Symbol	Min	Тур	Max	Unit
Supply voltage		V <sub>CC</sub>	4.75	5.00	5.25	V
Output voltage		V <sub>OH</sub>	—	—	5.5	V
Output current		I <sub>OH</sub>	—	—	-2.6	mA
		I <sub>OL</sub>	—	—	24	mA
Operating temperature		Topr	-20	25	75	°C
Enable pulse width	"H" Level	+	15	—	—	ns
Ellable puise width	"L" Level	t <sub>w</sub>	15	—	—	ns
Data setup time		t <sub>su</sub>	5↓	—	—	ns
Data hold time		t <sub>h</sub>	20↓	_	—	ns



### **Electrical Characteristics**

 $(Ta = -20 \text{ to } +75 \ ^{\circ}\text{C})$ 

Item	Symbol	min.	typ.*	max.	Unit	Condition		
	V <sub>IH</sub>	2.0	—		V			
Input voltage		_	—	0.7	V	Data inputs		
	V <sub>IL</sub>	_	_	0.8	v	G, Output control inputs		
	V <sub>он</sub>	2.4	_	_	V	$V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL max}$ $I_{OH} = -2.6 \text{ mA}$		
Output voltage				0.4		$I_{OL} = 12 \text{ mA}$ $V_{CC} = 4.75 \text{ V},$		
	V <sub>OL</sub>			0.4	V	$V_{CC} = 4.75 \text{ V},$ $I_{OL} = 24 \text{ mA}$ $V_{IH} = 2 \text{ V}, \text{ V}_{IL} = \text{ V}_{IL \text{ max}}$		
Outrast summary	I <sub>OZH</sub>	_	—	20		$V_{\rm O} = 2.7 \text{ V}$ $V_{\rm CC} = 5.25 \text{ V},$		
Output current	I <sub>OZL</sub>	_		-20	μA	V <sub>O</sub> = 0.4 V V <sub>IH</sub> = 2 V		
	IIН	_		20	μΑ	$V_{CC} = 5.25 \text{ V}, \text{ V}_{I} = 2.7 \text{ V}$		
Input current	Ι <sub>Ι</sub>	_		-0.4	mA	$V_{CC} = 5.25 \text{ V}, \text{ V}_{I} = 0.4 \text{ V}$		
	l <sub>l</sub>	_		0.1	mA	$V_{CC} = 5.25 \text{ V}, \text{ V}_{I} = 7 \text{ V}$		
Short-circuit output current	los	-30	_	-130	mA	V <sub>CC</sub> = 5.25 V		
Supply current	Icc	_	24	40	mA	$V_{CC} = 5.25 V,$ $V_{I} = 4.5 V$ (Output control)		
Input clamp voltage	V <sub>IK</sub>	_	_	-1.5	V	$V_{CC} = 4.75 \text{ V}, \text{ I}_{IN} = -18 \text{ mA}$		

Note: \*  $V_{CC} = 5 V$ , Ta = 25°C

### **Switching Characteristics**

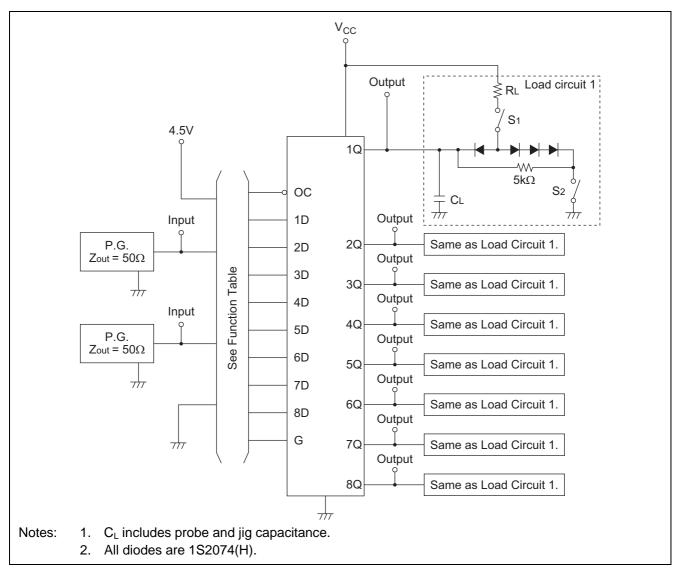
 $(V_{CC} = 5 V, Ta = 25^{\circ}C)$ 

Item	Symbol	Input	Output	min.	typ.	max.	Unit	Condition
Propagation delay time	t <sub>PLH</sub>	D	Q		12	18		
	t <sub>PHL</sub>	D	Q	—	12	18	]	
	t <sub>PLH</sub>	G	Q	—	20	30	ns	$\begin{array}{l} C_{L} = 45 \; pF, \\ R_{L} = 667 \; \Omega \end{array}$
	t <sub>PHL</sub>			—	18	30		
Output enable time	t <sub>ZH</sub>	ос	Q	—	15	28		
	t <sub>ZL</sub>	00		_	25	36		
Output disable time	t <sub>HZ</sub>	ос	Q	_	12	20		$C_L = 5 \text{ pF},$
	t <sub>LZ</sub>	00		_	15	25		$R_L = 667 \ \Omega$

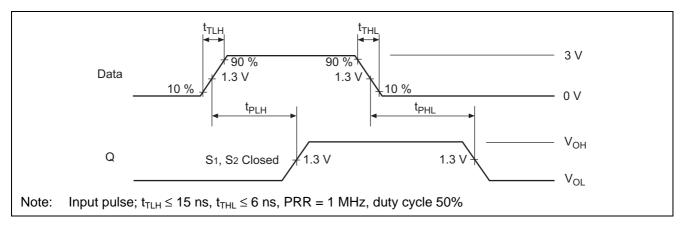


### **Testing Method**

#### **Test Circuit**

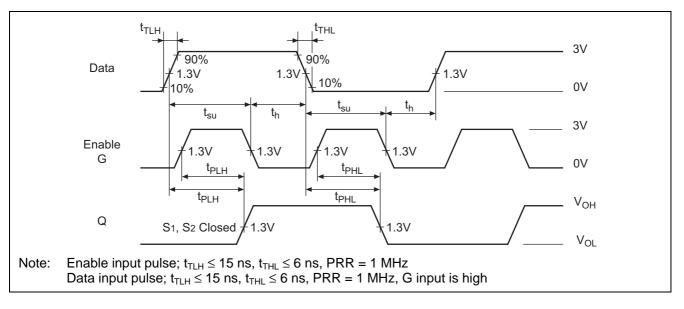


#### Waveforms 1

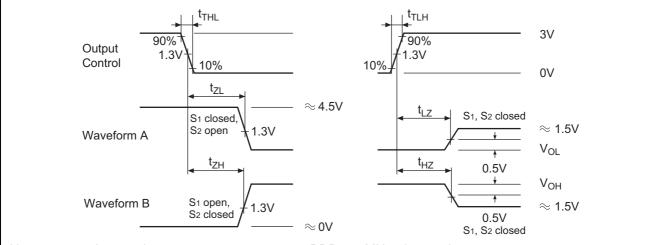




#### Waveforms 2



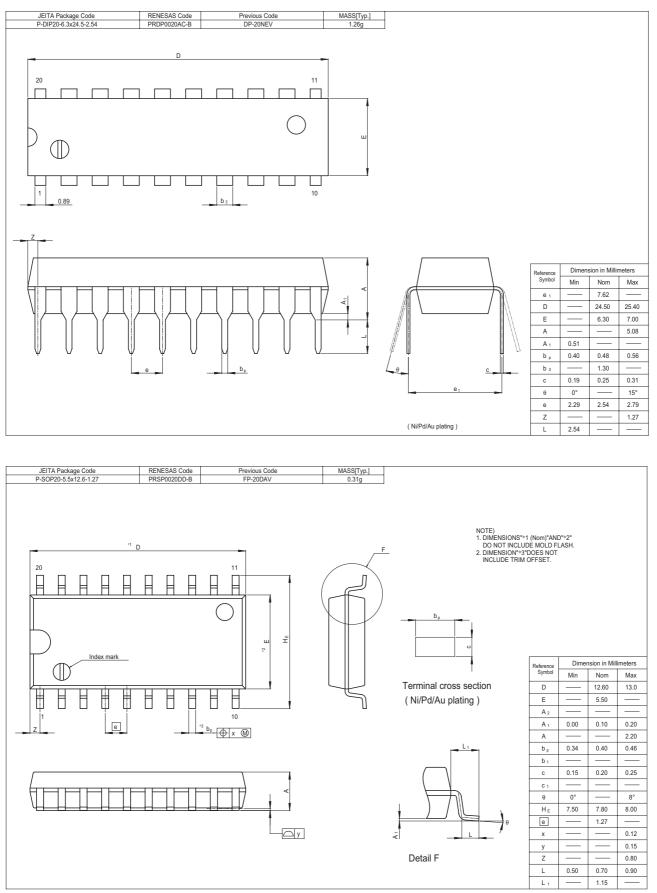
#### Waveforms 3



Notes: 1. Input pulse;  $t_{TLH} \le 15$  ns,  $t_{THL} \le 6$  ns, PRR = 1 MHz, duty cycle 50%

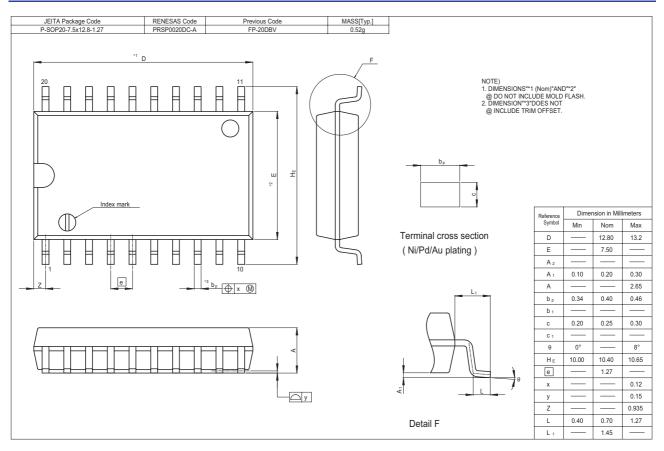
2. Waveform A if for an output with internal conditions such that the output is low except when disabled by the output control. Waveform B is for an output with internal conditions such that the output is high except when disabled by the output control.

#### **Package Dimensions**





#### HD74LS373





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