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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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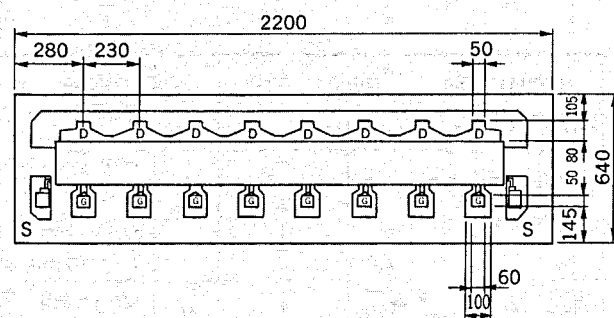
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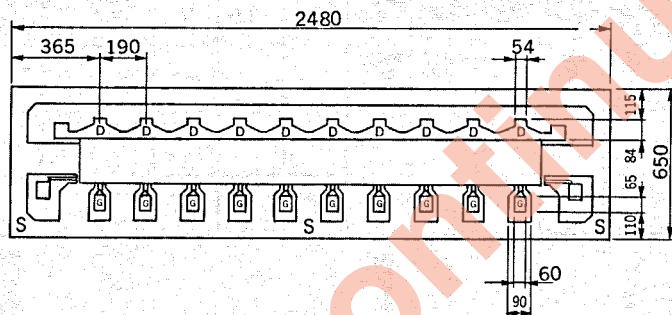
C-BAND POWER GaAs FET CHIPS N-CANNEL GaAs FET CHIPS

PHYSICAL DIMENSIONS (Units : μm)

NE004800



NE004100



DESCRIPTION

The NE004 series is power GaAs FET chips which offers high output power and high gain in the C-band. The gate length of the device is less than $1 \mu\text{m}$ to increase linear gain and the series employs PHS (Plated Heat Sink) technology to reduce the thermal resistance. The NE004800 consists of eight cells and the NE0041000 consists of ten cells. The NE0041600 is in a pair of the NE004800 and the NE0042000 is in a pair of the NE0041000. The 6 W output power can be obtained from these device combined by the external circuit.

FEATURES

- High output power
- Class A operation
- High power added efficiency

ORDERING INFORMATION

PART NUMBER	TYPICAL PERFORMANCE		
	$P_{O(1 \text{ dB})}$ (dBm)	G_L (dB)	USABLE FREQUENCY (GHz)
NE004800-6	34.8	10.0	5.9 to 6.4
NE004800-8	34.8	8.5	7.1 to 7.7
NE004100-6	35.3	9.5	5.9 to 6.4
NE0041600-6	37.3	9.0	5.9 to 6.4
NE004200-6	37.8	9.0	5.9 to 6.4

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

		NE004800	NE0041000	NE0041600	NE0042000	
Drain to Source Voltage	V_{DS}	20	20	20	20	V
Gate to Source Voltage	V_{GS}	-15	-15	-15	-15	V
Drain Current	I_D	2.5	3.0	5.0	6.2	A
Gate Current	I_G	20	25	40	50	mA
Total Power Dissipation	P_T^{*1}	25	25	50	50	W
Channel Temperature	T_{ch}	175	175	175	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65 to +175	-65 to +175	-65 to +175	-65 to +175	$^\circ\text{C}$

*1 $T_c = 25^\circ\text{C}$ ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	NE004800-6 NE004800-8			NE0041000-6			NE0041600-6			NE0042000-6			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Saturated Drain Current	I_{DSS}	1.5	2.0	2.5	1.5	2.3	3.0	3.0	4.0	5.0	3.0	4.5	6.0	A	$V_{DS} = 2.5\text{ V}$, $V_{GS} = 0$
Pinch-off Voltage	V_p	-4.0	-2.5	-1.5										V	$V_{DS} = 2.5\text{ V}$, $I_D = 10\text{ mA}$
					-4.0	-2.5	-1.5							V	$V_{DS} = 2.5\text{ V}$, $I_D = 14\text{ mA}$
								-4.0	-2.5	-1.5				V	$V_{DS} = 2.5\text{ V}$, $I_D = 20\text{ mA}$
											-4.0	-2.5	-1.5	V	$V_{DS} = 2.5\text{ V}$, $I_D = 27\text{ mA}$
Transconductance	g_m		750			1000								mS	$V_{DS} = 2.5\text{ V}$, $I_D = 0.8\text{ A}$
									1500			2000		mS	$V_{DS} = 2.5\text{ V}$, $I_D = 1.6\text{ A}$
Thermal Resistance	R_{th}			6			6			3			3	$^\circ\text{C/W}$	channel to heatsink

PERFORMANCE SPECIFICATIONS ($T_a = 25^\circ\text{C}$)

PART NUMBER	CHARACTERISTICS						TEST CONDITIONS			
	P_O (1 dB) (dBm)		G_L (dB)		P_{out} (dBm)	η_{add} (%)	I_{DS}^{*2} (A)	V_{DS} (V)	P_{in}^{*3} (dBm)	frequency (GHz)
	MIN.	TYP.	MIN.	TYP.	TYP.	TYP.	MAX.			
NE004800-6 * ⁶	34.5	34.8	9.5	10.0	35.3	36	1.3	9	28	5.9 to 6.4
NE004800-8 * ⁶	34.5	34.8	8.0	8.5	35.3	31	1.3	9	29	7.1 to 7.7
NE0041000-6 * ⁶	35.0	35.3	9.0	9.5	35.8	39	1.3	9	28	5.9 to 6.4
NE0041600-6 * ⁴ , * ⁶	37.0	37.3	8.5	9.0	37.8	34	2.6	9	31	5.9 to 6.4
NE0042000-6 * ⁵ , * ⁶	37.5	37.8	8.5	9.0	38.3	37	2.6	9	32	5.9 to 6.4

*2 The maximum value of I_D at P_O (1 dB) point*3 Condition for P_{out}

*4 The device consists of a pair of NE004800-6 chips

*5 The device consists of a pair of NE004200-6 chips

*6 Sampling basis of 2 points on a wafer (Accept : 0/Reject : 1)

CHIP HANDLING**DIE ATTACHMENT**

Die attach can be accomplished with a Au-Sn (300 ± 10 °C) preforms in a forming gas environment. Epoxy die attach is not recommended.

BONDING

Gate and drain bonding wires should be minimum length, semi-hard gold wire(3–8 % elongation) 30 microns or less in diameter.

Bonding should be performed with a wedge tip that has a taper of approximately 15 %. Die attach and bonding time should be kept to a minimum. As a general rule, the bonding operation should be kept within a 280 °C – 5 minute curve. If longer periods are required, the temperature should be lowered.

PRECAUTIONS

The user must operate in a clean, dry environment. The chip channel is glassivated for mechanical protection only and does not preclude the necessity of a clean environment.

The bonding equipment should be periodically checked for sources of surge voltage and should be properly grounded at all times. In fact, all test and handling equipment should be grounded to minimize the possibilities of static discharge.

Discontinued Product

Discontinued Product