Microcomputer Technical Information

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IE-789860-NS-EM1 Emulation Board for μPD789860, μPD789861, μPD789052, μPD789062 Subseries Usage Restrictions		Document No.	SBG-DT-04-0124	1/2
		Date issued	April 2, 2004	
		Issued by	Microcomputer Group 2nd Solutions Division Solutions Operations Unit NEC Electronics Corporation	
Related documents	IE-789860-NS-EM1 User's Manual: U16499EJ1V0UM00 (1st edition)	Notification classification	√	Usage restriction
				Upgrade
				Document modification
				Other notification

1. Affected product

IE-789860-NS-EM1 Control code[Note]: A, B, C, D

Note The "control code" is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased. If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.

2. Details of restriction

The following bug has been added. See attachment 1 for details.

- No.5 Bug in EEPROM guard function

3. Workaround

See attachment 1 for details.

4. Modification schedule

Products in which No.5 is modified are scheduled for release as follows.

Newly shipped products: From the shipment at the end of July 2004 (control code: E)

Upgrade for already shipped products: Available from late June, 2004

* Note that this schedule is subject to change without notice. For the detailed release schedule of modified products, contact an NEC Electronics sales representative.

5. List of restrictions

Notes on Using IE-789860-NS-EM1, including the revision history and detailed information, is described in the attachment.

6. Document revision history

IE-789860-NS-EM1 Emulation Board for μPD789860, μPD789861, μPD789052, μPD789062 Subseries Usage Restrictions Revision History

Document Number	Date Issued	Description
SBG-T-1811-E	October 22, 1999	Addition of bug (No.1)
SBG-T-2104-E	July 21, 2000	Addition of bug (No.2)
SBG-DT-04-0124 (This document)	April 2, 2004	Addition of bug (No.5)

Notes on Using IE-789860-NS-EM1

1. Product Version

Product name: IE-789860-NS-EM1

Control Code[Note]	Remark
A	I/O EVA chip μPD78E9860 1.0
B	I/O EVA chip μPD78E9860 1.1
C	I/O EVA chip μPD78E9860 1.3
D	I/O EVA chip μPD78E9860A 1.0/μPD78E9861A 1.0

Note The "control code" is the second digit from the left in the 10-digit serial number starting with E (if it has not been upgraded). If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.

2. Product History

No.	Bugs and Changes/Additions to Specifications	Control Code			
		A	B	C	D
1	Bug when a non-maskable interrupt via the key return signal is used	×	√	√	√
2	Bug in key return signal operation	×	×	√	√
3	Addition of support for the μPD789052, μPD789062 Subseries	–	–	–	√
4	Modification of specification of 8-bit timers 30 and 40	–	–	–	√
5	Bug in EEPROM guard function	×	×	×	×

×: Applicable, √: Not applicable (change of specification), –: Not relevant

3. Details of Bugs and Additions to Specifications

No.1 Bug when a non-maskable interrupt via the key return signal is used

[Description]

Because the interrupt request signal of the emulation chip is not cleared when a non-maskable interrupt via the key return signal is used, other interrupts cannot be acknowledged.

[Workaround]

Refer to the attachment.

This bug has been corrected in IE-789860-NS-EM1 control code B.

No.2 Bug in key return signal operation

[Description]

The key return interrupt (INTKR1) should be generated by the input of the falling edge of P40/KR10 to P43/KR13, but is inadvertently generated by a low-level input.

[Workaround]

There is no workaround.

This bug has been corrected in IE-789860-NS-EM1 control code C.

No.3 Addition of support for the μPD789052, μPD789062 Subseries

[Description]

The μPD789052, μPD789062 Subseries is supported in IE-789860-NS-EM1 control code D or later.

[Caution]

Use the device file DF789062 (E1.00e (July 5, 2002) or later).

No.4 Modification of specification of 8-bit timers 30 and 40

[Description]

The carrier generator output control register 40 (TCA40) has been changed from write-only (W) to read/write (R/W) in IE-789860-NS-EM1 control code D or later due to the specification change in the target device.

[Caution]

Use the device file DF789861 (E1.10c (May 31, 2002) or later) or DF789062 (E1.00e (July 5, 2002) or later).

No.5 Bug in EEPROM guard function

[Description]

A guard break occurs when an instruction that selects the output of 8-bit timer 40 as the count clock (data write time) of the EEPROM timer is executed and reading the EEPROM is enabled (ERE10 = 1) after the operation of 8-bit timer counter 40 is stopped.

```
Example 1  MOV EEWC10,#68H      ; Selects EEPROM timer count clock
           SET1 ERE10           ; Enables EEPROM read

Example 2  MOV EEWC10,#68H      ; Selects EEPROM timer count clock
           MOV EEWC10,#6CH      ; Enables EEPROM read
```

[Workaround]

Implement (1) or (2) below.

(1) Do not stop the operation of 8-bit timer counter 40 when enabling EEPROM read using the instruction in **Example 1** or **Example 2**.

(2) When enabling EEPROM read while the operation of 8-bit timer counter 40 is stopped, select the count clock for the EEPROM timer and enable EEPROM read using one instruction.

```
Example 3  MOV EEWC10,#6CH      ; Enables EEPROM read at the same time as selecting
                                  EEPROM timer count clock
```

This bug will be corrected in IE-789860-NS-EM1 control code E.

4. Cautions

(1) An RC oscillator cannot be emulated by the IE-789860-NS-EM1. Only the oscillator functions described in the user's manual can be emulated.

(2) When emulation of the low-voltage detector and power-on-clear circuit detection voltage is performed, it is affected by voltage fluctuation and noise. Therefore, the detected voltage must be checked in the EEPROM product.

(3) When a program that illegally accesses EEPROM is executed in the IE-789860-NS-EM1, an error message is displayed and a break occurs. The conditions for illegally accessing the EEPROM and the displayed error message are described below.

Illegal Access Condition

Error message: **Unspecified Illegal**	
EEPROM illegal access conditions	
<1>	Write instruction to EEPROM is executed when EWE10 = 0.
<2>	Write instruction to EEPROM is executed while the clock selected by EEPROM is stopped.
<3>	Write instruction to EEPROM is executed while EEPROM is being written to.
<4>	Read instruction from EEPROM is executed while EEPROM is being written to.
<5>	Instruction is fetched from EEPROM while EEPROM is being written to.
<6>	EWE10 is cleared to 0 while EEPROM is being written to.
<7>	ERE10 is cleared to 0 while EEPROM is being written to.
<8>	Main clock is stopped while EEPROM is being written to.
<9>	Count clock selection of the write time setting timer is changed while EEPROM is being written to.
<10>	RESET is applied while EEPROM is being written to.

(4) The IE-789860-NS-EM1 includes a POC switching circuit, which is used to control the power-on-clear circuit function via software. Set this circuit to on/off using an SFR.

(5) The oscillation stabilization wait time after STOP mode release by $\overline{\text{RESET}}$ input or reset release using POC is fixed to $2^7/f_X$ in the IE-789860-NS-EM1. Only the mask option functions described in the user's manual can be emulated.

(6) Data can be read from EEPROM even if ERE = 0 (read disabled).

(7) No error occurs even if the time for writing to EEPROM is set outside the range of 3.6 to 6.6 ms.

(8) Procedure for setting ERE10 and EWE10 when writing to EEPROM

<1> Set ERE10 to 1.

<2> Set EWE10 to 1.

<3> Insert a wait of 1 ms or more by software (no error occurs even if the wait period is within 1 ms).

<4> Writing to the EEPROM is enabled.

Workaround for No.1 in Bugs and Changes/Additions to Specifications:

The interrupt request signal of the emulation chip is cleared when the EI instruction has been executed. Therefore, be sure to execute the EI instruction in the vector table if the non-maskable interrupt of the key return signal is used. At this time, the interrupt servicing of the key return signal is executed two times, and therefore, processing that returns as soon as servicing the interrupt is started the second time is necessary. Here is an example of software.

Example:

```
 (Main routine)
        •
        •                               ; Clears interrupt counter
        MOV         B,#0
        STOP
        •
        •
(Key return interrupt vector routine)
VINTKR:
        INC         B                   ; Increments interrupt counter
        EI                              ; Clears interrupt request flag for emulation
        MOV         A,B
        CMP         A,#02H              ; First interrupt?
        BZ          $KR_END0            ; Return processing if interrupt is second interrupt
        •
        •
        •           Original processing
        •
        •
        BR          $KR_END1
KR_END0:
        MOV         B,#0
KR_END1
        RETI
```

<Flow of operation in this example>

STOP instruction execution

Occurrence of non-maskable interrupt because of key return

Branch to vector of key return

Incrementing counter (B ← 1)

EI instruction execution (kept pending while non-maskable interrupt is serviced)

Execution of original processing because interrupt is first interrupt (B = 1)

Return to main routine (pending EI instruction is executed at this point and execution branches to vector of key return again)

Increments counter (B ← 2)

Clears counter and branches to return processing because interrupt is second interrupt (B = 2)