NEC

Customer Notification

VR7701™

64-bit Microprocessor

Operating Precautions

µPD30671F2-400-UA5-A

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✓ : Not applicable
✗ : applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product. R2.0 are only available as ES and are marked accordingly.

(B) Description of Operating Precautions

No. 1	Address stored in BadVAddr register in case of an address error (Specification change notice)

	Details
	A branch or jump instruction must not be placed two instructions before an address error boundary as shown below:
	`instruction n:  branch instruction`
	`instruction n+1:  any instruction`
	`<---- address error boundary`
	`instruction n+2:  any instruction`
	Note: An address error boundary is the boundary between an address range where access is legal and an address range, where access is illegal (for example: boundary between user and kernel segments, when the processor is in user mode.

No. 2	Boundary scan function for PCI-X pins (Specification change notice)
	Details All PCI-X pins are excluded from the boundary scan chain.

No. 3	Debug register initialization (Specification change notice)
	Details The MRST bit in the DM_CONTROL register must be set to “1” in order to avoid resetting of the MON_DATA register by a RESET# input. This is only required when the processor is running in debug mode and the N-Wire ICE software takes care of this specification change.

No. 4	Debug trigger and simultaneous address error exception (Specification change notice)
	Details If the processor is running in debug mode and if a debug trigger and an address error (or TLB) exception occur in the same instruction, `0xbc001000` (the debug exception vector) is used as the exception vector, however the exception code in the CAUSE register indicates an address error (or TLB) exception. This situation occurs only if • the data break control register is set only for generating a trigger and not for generating a break • the debug trigger and simultaneous address error (or TLB) exception are generated by a load/store instruction. This phenomenon does not affect the operation in normal mode.

No. 5	NMI masking function in debug mode (Specification change notice)
	Details An NMI request, that is already held internally, occurs in debug mode, even when NMI exception masking is activated in the DM_CONTROL register. This phenomenon does not affect the operation in normal mode. The N-Wire ICE software takes care of this specification change.

No. 6	PCI-X buffer output impedance (Direction of usage)
	Details Series resistors of 10 O, ± 15% are required in each PCI-X line of the VR7701 in order to fulfill the electrical specification for PCI-X.

No. 7	Ethernet data loss after 500 Bytes of reception (Specification change notice)
	Details To avoid data loss on Ethernet reception via DMA, one of the following rules must be implemented: 1. The buffer address of the receive buffer must be word-aligned (32 bits) and the buffer size must be a multiple of 4. 2. The sum of the 4 LSBs of the receive buffer address and the 4 LSBs of the buffer size must be a multiple of 4. 3. The buffer size in the receive descriptor must be set to 511 or less.

No. 8	BIUEVTYPE1/2 register setting (Specification change notice)
	Details Setting values between 0y000001 and 0y010101 in the 6 LSB positions of the BIUEVTYPE1/2 registers is prohibited.

No. 9	MI1/2MD signal output delay specification (Specification change notice)
	Details The MI1MD and MI2MD signals have a minimum output delay time ($t_{DO\ MD}$) of 5 ns.

No. 10	INT_ACT_LV register setting (Specification change notice)
	Details Access to the INT_ACT_LV register is prohibited. Consequently, all external interrupts INTP(7:0) can only be used as active-high level interrupts.

No. 11	SDTIMING register setting (Specification change notice)
	Details Setting 0y111 (for a CAS latency of 3.5) in the TCL field of the SDTIMING register – is prohibited. Consequently the use of registered DDR-SDRAM DIMM modules with a CAS-latency of 2.5 for the memory chips – and thus, an effective CAS latency of 3.5 for the memory modules – is not supported.

No. 12	PCI-X initialization pattern AC specification (Specification change notice)
	Details VR7701 requires a minimum hold time of 2 ns with respect to the rising edge of PRST#, if an external device drives the PCI-X initialization pattern.

No.13	Configuration Read data in case of Master Abort (Direction of usage)

Details

In case of a Master Abort as response to a Configuration Read (occurs, if no other PCI device responds with DEVSEL to the Configuration Read), the Configuration Read data is not fixed to 0xffff ffff. Therefore the presence of external devices must be tested by checking the RMA bit in the PCI Error Status register.

No. 14	Secondary cache parity generation (Direction of usage)

Details

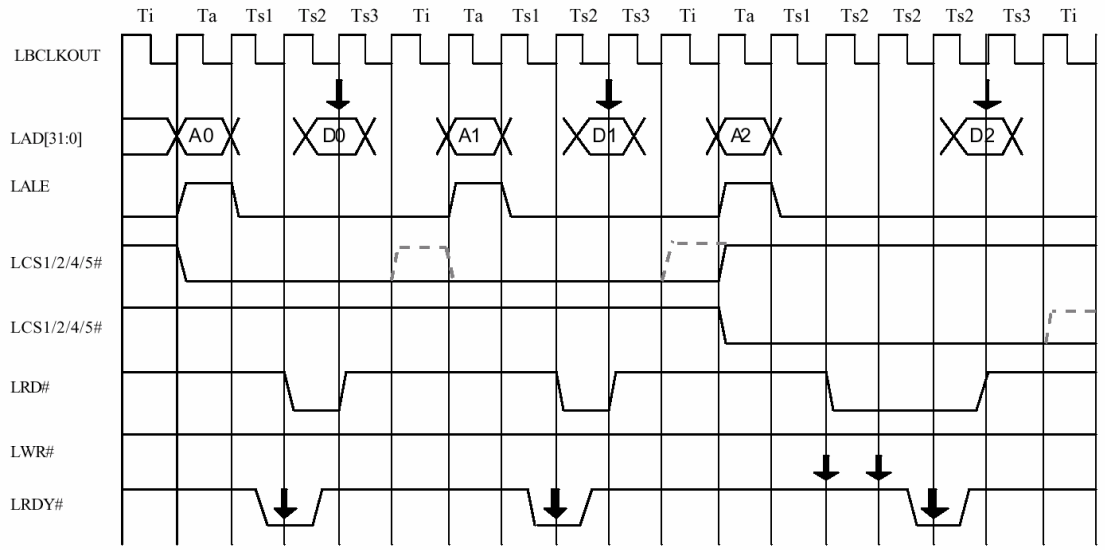
For the first time after reset, when a write from CPU Core to secondary cache or a DMA from OnChipBus to secondary cache is performed, the following rule must be maintained:

- mask NMI CH5 by setting bit 4 in NMI_MASK register to “0”
- execute dummy write to secondary cache
- clear parity error interrupt by writing “1” to bit 4 of the NMI_CLR register
- unmask NMI CH5 by setting bit 4 in NMI_MASK register to “1”

No. 15	Local bus interface CS timing (Specification change notice)

Details

Local bus chip select signals LCS1, LCS2, LCS4 and LCS5 retain their previous value during local bus idle cycles. The figure below illustrates this behavior; the dotted lines show the originally specified behavior.



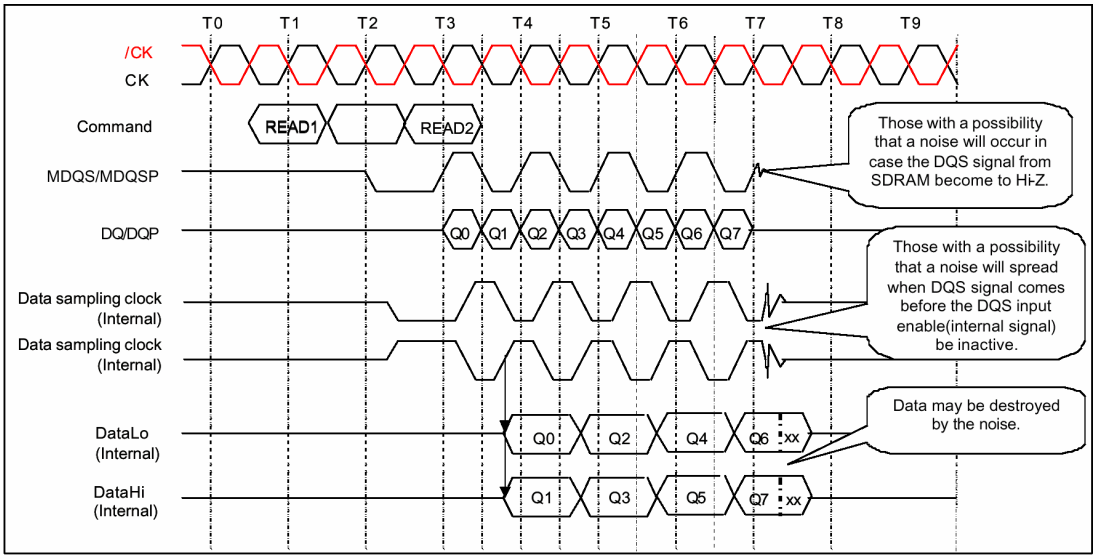
No. 16	BIU write operation (Specification change notice)
	Details Write data from the CPU core to 2nd level cache may overwrite write buffer data under certain circumstances. To avoid this situation, the following setting has to be made: • set O3RETURN# pin of VR7701 to high level (i.e. switch O3-Return mode off) or and set EM bits in CONFIG register to 0y10 (pipeline write mode). **Note:** The O3RETURN# pin will be documented from the next revision of the VR7701 User's Manual (U1633416334EJ2V0UM00) onwards. Currently, O3RETURN# is described as GND pin Y4.

No. 17	SDR-SDRAM support (Specification change notice)
	Details SDR (**s**ingle **d**ata **r**ate) SDRAM support is deleted from the VR7701 specification. DDR-SDRAM is supported exclusively.

No. 18	MMD(63:0), MMDP(7:0), MDQS(7:0) and MDQSP signal termination (Specification change notice)

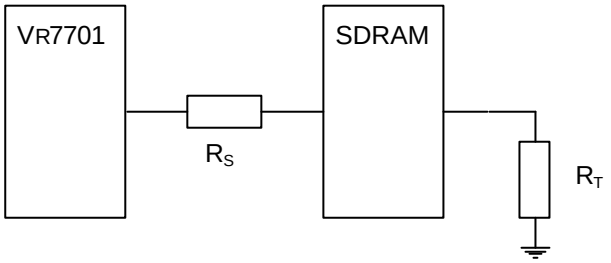
Details

Noise on the MMD(63:0), MMDP(7:0), MDQS(7:0) and MDQSP pins may destroy memory read data as illustrated in below diagram.

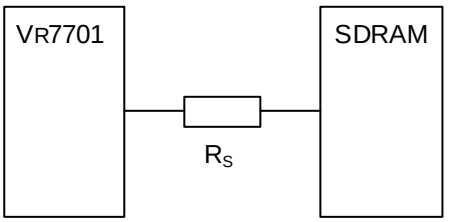


To reduce the noise the following alternatives to standard termination of DDR-SDRAM data lines are recommended:

a) a termination with a resistor to GND (instead of V_{TT}) for MMD(63:0), MMDP(7:0), MDQS(7:0) and MDQSP signals



b) no termination at all for the MMD(63:0), MMDP(7:0), MDQS(7:0) and MDQSP signals,.



In any case the user must check using transmission simulation techniques, whether the circuitry does not violate any VR7701 specifications. These simulations must take the influence of the PCB layout into account. They may as well result in other alternatives to standard DDR-SDRAM data line termination, which are acceptable as long as no spec is violated.

(C) Valid Specification

Item	Date published	Document No.	Document Title
1	August 2003	U16395EJ2V0DS00	VR7701 Data Sheet
2	October 2003	U16334EJ3V0UM00	VR7701User's Manual

(D) Revision History

Item	Date published	Document No.	Comment
1	December 2003	TPS-HE-B-6202-1	initial release
2	March 2004	TPS-HE-B-6202-2	Change description of item 11
3	April 2004	TPS-HE-B-6202-3	Change description of workaround for item 18